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A NOVAL DYNAMIC CALIBRATION APPROACH FOR CURRENT-STEERING DACS

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ABSTRACT

With increasing applications in telecommunication systems, high speed and high accuracy digital-to-analog converters(DAC) are becoming more and more important. Of particular interest is the dynamic performance at high frequencies. The dynamic performance is often characterized by the spurious free dynamic range (SFDR) and this is limited by the spectral harmonics that are mainly attributable to system nonlinearities. In this paper, the dynamic nonlinearity in the time domain is analyzed and its affect on the output waveform is discussed. A novel approach is presented to calibrate the dynamic errors. The validity of this approach is demonstrated with a 10-bit current steering DAC. Simulation results show that the nonlinear harmonics can be dramatically reduced and SFDR can be correspondingly improved by using this calibration scheme.

1. INTRODUCTION

In signal processing and telecommunication systems, the digital-to-analog converter is often used to reconstruct an analog signal from an arbitrary digital waveform. This key part often limits the accuracy and speed of the overall system. Several different architectures are used to build the DACs. Among them, the resistor-loaded current-steering DAC is almost exclusively used when high speed and high accuracy are required. In communication applications, DAC quality is often determined by the high frequency spectral purity of the output signal and this is dominantly determined by the nonlinearities of the DAC. The spurious free dynamic range (SFDR) is a widely used measure for the linearity of the converter [1].

SFDR is degraded by both static and dynamic nonlinearities. The major static error sources are due to mismatch between current sources and their finite output impedance. These error sources cause inaccurately settled values for DAC outputs. The current source mismatch is mainly due to the random variations that can be attributed to local random variations and gradient effects [2]. Special layout and placement techniques, such as common centroiding, judicious switch sequencing, and Q^2 random walks [3][4][5] can be used to reduce these effects. Even if the current sources are perfectly matched; the output current of the current sources may still vary with the output voltage because the output impedance of the current sources is not infinite. Strategies do exist for improving the output impedance. For example, cascoded current sources and current-steering switches can be used to increase the output impedance. For video and wireless telecommunication applications, both static linearity and dynamic linearity are important. Both static and dynamic nonlinearities contribute to undesired harmonics in the output.

Many calibration approaches [2][5][6] have been reported in the literatures for improving DAC performance. Most of them focus only on improving the static nonlinearity calibration. In higher frequency ranges, little has been reported that deals with dynamic calibration [7]. Some modest improvements in high frequency SFDR have been reported with return-to-zero structures (RTZ) but this improvement has been obtained by sacrificing half of the signal power.

In this paper, a novel dynamic DAC nonlinearity calibration approach is proposed that can improve high frequency SFDR without attenuation of the output signal power. Simulation results from a prototype 10-bit current-steering DAC are used to validate this approach. .

The paper is organized as follows: the time domain analysis and calibration approach are discussed in Section 2; the DAC structure and simulation results are presented in Section 3; conclusions are given in Section 4.

2. TIME DOMAIN ANALYSIS AND CALIBRATION

The output of a DAC with linear transfer characteristics, normalized by the size of the transition, is depicted in Fig.1 for under-dampedand over-damped settling. Although the outputs differ considerably from ideal steps at the leading edge of the transitions, these nonidealies do not create any significant harmonics in the output waveform.

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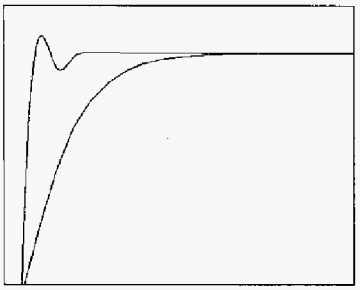


Fig.1 Different output waveforms of step response

In a real DAC, the settling is not perfectly linear and the value to which the DAC settles may be incorrect. These nonidealities contribute to both static and dynamic nonlinearity thus causing distortion in the output. Static nonlinearities are dominantly attributable to nonlinear settling artifacts in the output such as insufficient settling time, timing skew, slewing and glitches as shown as Fig 2(a).

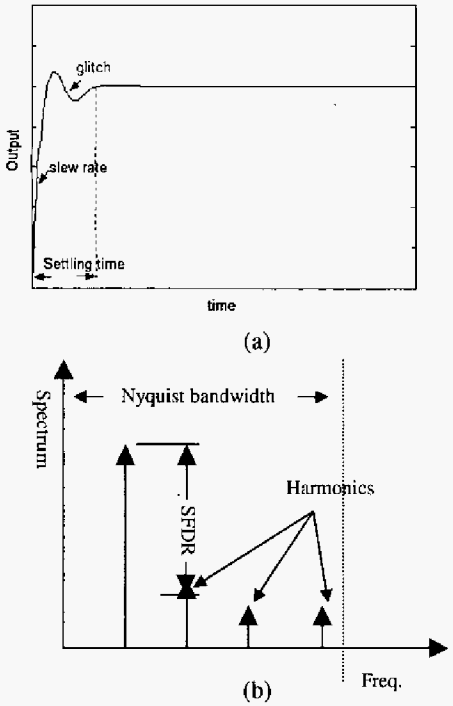


Fig. 2 dynamic nonlinearities
(a) time domain (b) frequency domain

Most of these occur at the early in the transition period. As the input signal frequency increases or the sampling frequency increases, the dynamic nonlinearity components becomes larger, so the linearity degrades and the magnitude of SFDR decreases. In order to improve the SFDR of the DACs, the effects of the dynamic nonlinearities must be reduced. Cong [2] improved low and high frequency SFDR with very low power and small area. But the approach is good at low frequency; the SFDR still degrades with increasing frequency. Bugeja's structure [7] increased better dynamic linearity at high frequency by using "attenuate and track" approach. But this improvement is at the price of a factor of 2 in the signal power. However, we can get hint from this approach that the improvement in dynamic linearity of this approach is primarily due to the suppression of the prior code dependence. So measures can be adopted to improve the dynamic linearity without lose of signal power.

The dynamic distortion is caused by the nonlinear behavior of the DAC. The nonlinear behavior is considered to be a function of the input sequence. Assuming the ideal input sequence is A_0, A_1, ..., A_n, A_{n+1}, ... so the errors E can be expressed as

$$E=f(A_0, A_1, \ldots, A_n, A_{n+1}, \ldots)$$

This is a general expression. For most DACs, the error are primarily attributable to two successive input codes, for example, at the transition of A_n and A_{n+1}, $E=f(A_n, A_{n+1})$. So for the difference between A_n and A_{n+1}, an appropriate amount of current ΔI_n with time interval Δt can be generated and added to the raw DAC output to compensate the errors.

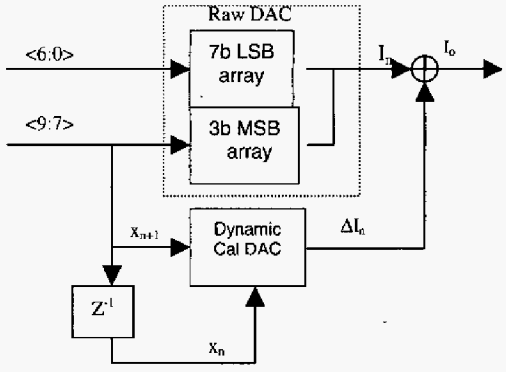
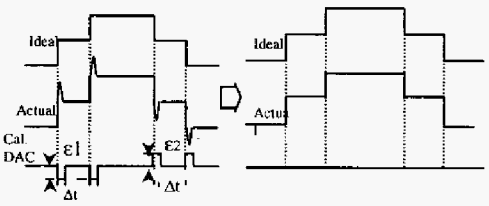


Fig.3 10 bit calibration scheme

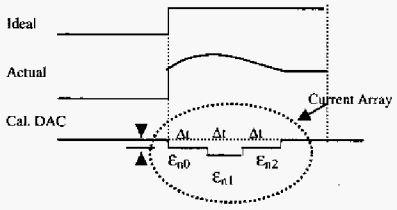
Fig.3 is the architecture of a 10-bit DAC. It consists of a needed calibrated raw DAC, a Dynamic Calibration DAC and a Delay block. The raw DAC is segmented into a 3-bit most significant bit (MSB) part and a 7-bit least significant bit (LSB) part. The thermometer decoding is used in the MSB part to reduce the effect of output glitches. The 7 bits LSB part is implemented with a binary structure. Because most of the nonlinearity errors come from the MSB part, the calibration is just applied to this part. The delay block is used to get two successive input codes: current input code A_n and next code A_{n+1}.

The dynamic calibration DAC will judge the difference between A_n and A_{n+1} to generate an current ΔI_n to the raw DAC. Then the desired output current I_0 can be gotten by summing I_n and ΔI_n.

Fig.4 is the conceptual illustration of the MSB calibration. Because of the nonlinearity, glitches exist during the transition period. If a waveform that is a vertical flip of the glitch can be generated and added to the output waveform at each transition period, the glitches can be canceled perfectly. But it is hard to generate such an analog waveform, so a digital pulse is used to compensate the glitch. The width and the



(a)



(b)

Fig.4 MSB calibration conceptual illustration

magnitude of the pulse can be set as Δt and ε respectively. A pulse array with the same Δt but different magnitudes ε_{ni} (I=0,1,2,...,k) as shown in Fig.4 (b) can be adopted for each step response to achieve a precisely calibration. Each pulse is a Δt delay relative to the previous one. For simplicity, just one pulse is used to compensate the glitch for every MSB code changing in this paper. ε, the magnitude of the pulse, is related to the difference between A_n and A_{n+1}. For each step height, there is a corresponding ε value to compensate the glitch. So a look-up-table can be used to save the calibration pulse magnitude values. After the calibration, the nonlinearity can be reduced and the SFDR can be improved.

It is assumed that all the compensation pulses are with the same width Δt. For the rise edge, the unit pulse height is ε_1 , it means that if the difference $\Delta A = A_n - A_{n+1}$ is 1, then the pulse's height is ε_1, while it will be $n\varepsilon_1$ if $\Delta A=n$. For the fall edge, the unit pulse height is ε_2. Fig.5 is the conceptual illustration of how to optimize the compensation pulses height for a given pulse width. First, keeping ε_2 fixed and varying ε_1, measuring the SFDR values for different ε_1. ε_1 will keep changing more at the same direction if the magnitude of SFDR increases, while changing ε_1 at the opposite direction if the magnitude of SFDR decreases. A local optimization point can be gotten for ε_1 by doing in this way. Then fixing ε_1

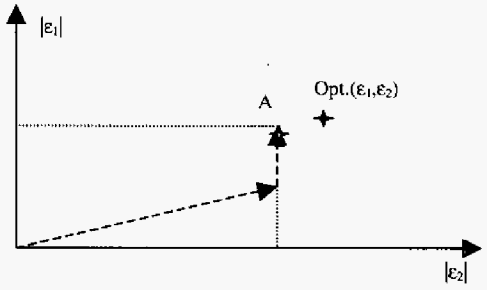


Fig.5 Parameters optimization illustration

and varying ε_2 , the local optimized value for ε_2 can be obtained. The optimization group values (ε_1, ε_2) for a given Δt can be gotten by alternatively optimizing ε_1 an d ε_2 for several times. The pulse width Δt can be optimized in the same way too. Then the optimization group values (ε_1, ε_2 , Δt) can be obtained for calibration.

3. SIMULATION RESULTS

Fig.6 is the test structure for 10-bit DAC that is segmented into a 3-bit MSB DAC and a 7-bit LSB DAC. An ideal ADC is used to generate the input code. The 7-bit LSB DAC is implemented with AHDL behavior model. The clock frequency is 100MHz. A low pass filter is used to remove the frequency outside the Nyquist band. The quantization error is removed to lower the noise floor, therefore, to make the harmonics explicit. This is valid because just the relative change of the harmonics before and after calibration is needed to be observed.

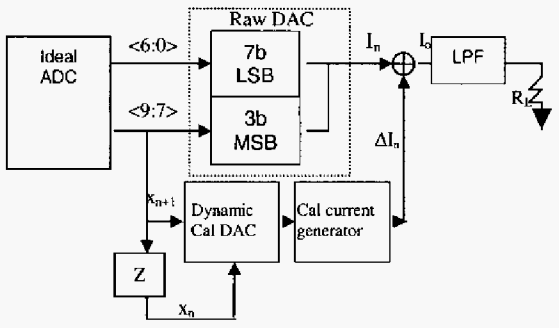


Fig. 6 10 bits DAC test structure

Fig. 7 is the current source structure. Fig.7 (a) is the normal current source and Fig.7 (b) is the cascoded current source.

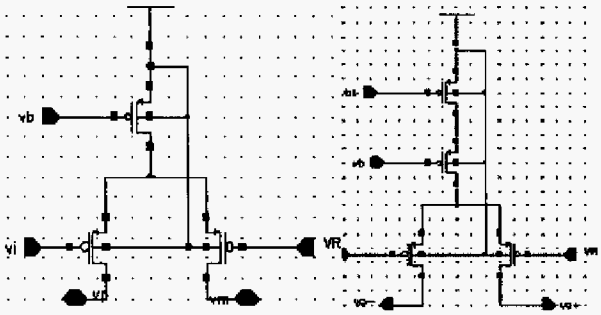


Fig.7 Current sources (a) normal (b) cascoded

Fig.8 is the plots of SFDR for the DAC with and without calibration by using normal current source as Fig.7 (a). It can be seen that the SFDR without calibration is below 40 dB when the frequency is higher than 20MHz. The SFDR is near 70dB after calibration. The improvement is about 30dB.

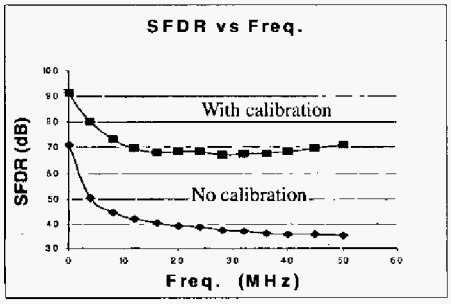


Fig.8 SFDR vs. input signal frequency normal current source

As mentioned in section 1, a cascaded current structure like Fig.7 (b) can be used to improve the SFDR by increasing the current cell output impedance. Fig.9 is the plot of SFDR for the DAC with and without

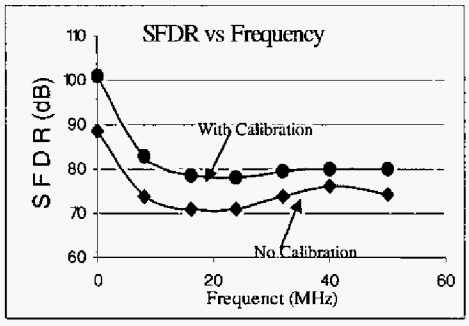


Fig.9 SFDR vs. input signal frequency cascoded current source

calibration by using cascoded current source. The SFDR is about 70dB and 80db respectively before and after calibration is when the frequency is higher than 20MHz. The improvement is about 10dB.

4. CONCLUSION

This paper presents a technique for DAC dynamic nonlinearity calibration. The dynamic errors are assumed to be a function of the two successive input digital codes. A 10-bit current steering DAC is designed to verify the validity of this approach. The simulation results show that generating an appropriate amount of current pulse and adding it to the raw DAC output current at each transition period can dramatically attenuate the input code dependence.

Only one current pulse is employed for each MSB transition during the calibration. So the error waveform caused by dynamic nonlinearity can't be completely compensated. If a current array is applied for each MSB transition, it will compensate nonlinearity more precisely, therefore achieve a better dynamic performance.

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